ELE 582 - Final Project Report

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1. Overview of the Circuit

Specification	Results
1.2V Power Supply	1.2 V
DC Power Consumption < 50 mW	25.34 mW
Transimpedance Gain > Ω	4,310.38* Ω
Bandwidth > 5 GHz	6.988 GHz
Gain Flatness < 1 dB	0.8848 dB
Differential Output Swing > 100 mV	43.1038
Input-referred Noise Current < $50pA/\sqrt{Hz}$	82.5 $pA/\sqrt{Hz}$
Input of Single-ended Photodiode w/ 0.5 pF Capacitance	✓
Differential Outputs w/ Transmission Line Loads	✓

*Transimpedance gain before differential stage is about 11,700

As shown in Figure 1, our transimpedance amplifier circuit has three main stages: input, amplification, and output. We will talk about each stage more in depth below.

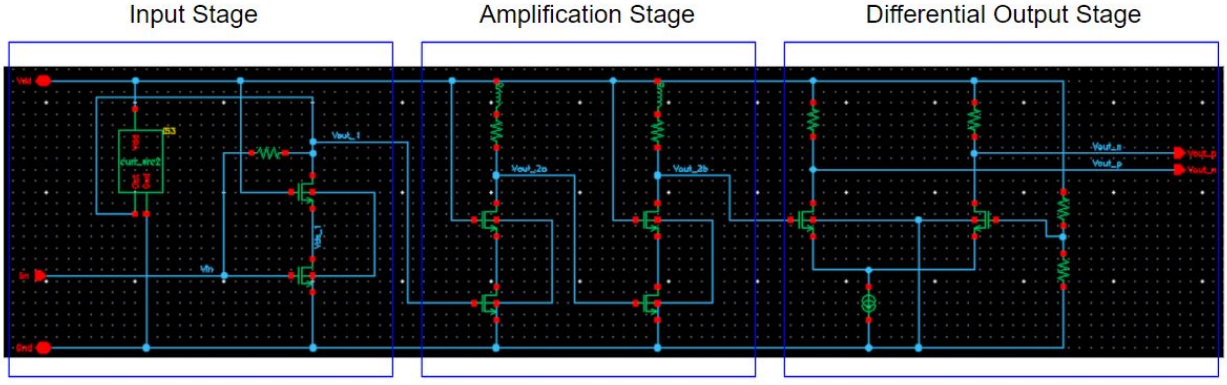

Figure 1: Full Trans-impedence Amplifier Circuit

2. Transimpedance Stage

2.1. Analytical Analysis of the Circuit

Our first stage converts the current input to an output voltage. Our circuit for this stage, as shown in Figure 2 (a), is inspired by the Cherry-Hooper design from Problem Set 3. Our design differs in that it uses a cascode-like topology. The cascode eliminates any direct parasitic paths between the input and output, thus suppressing the Miller effect. Since the largest capacitance in the system is the 50pF input capacitance, we require a small input impedance for good high frequency behavior. This design has an input impedance of approximately $1/g_{m1}$, which is about $100\,\Omega$ to $300\,\Omega$. The transimpedance gain of this topology is, approximately, $-R_f$. This allows us to easily obtain transimpedance gains between $100\,\Omega$ and $1\text{k}\,\Omega$.

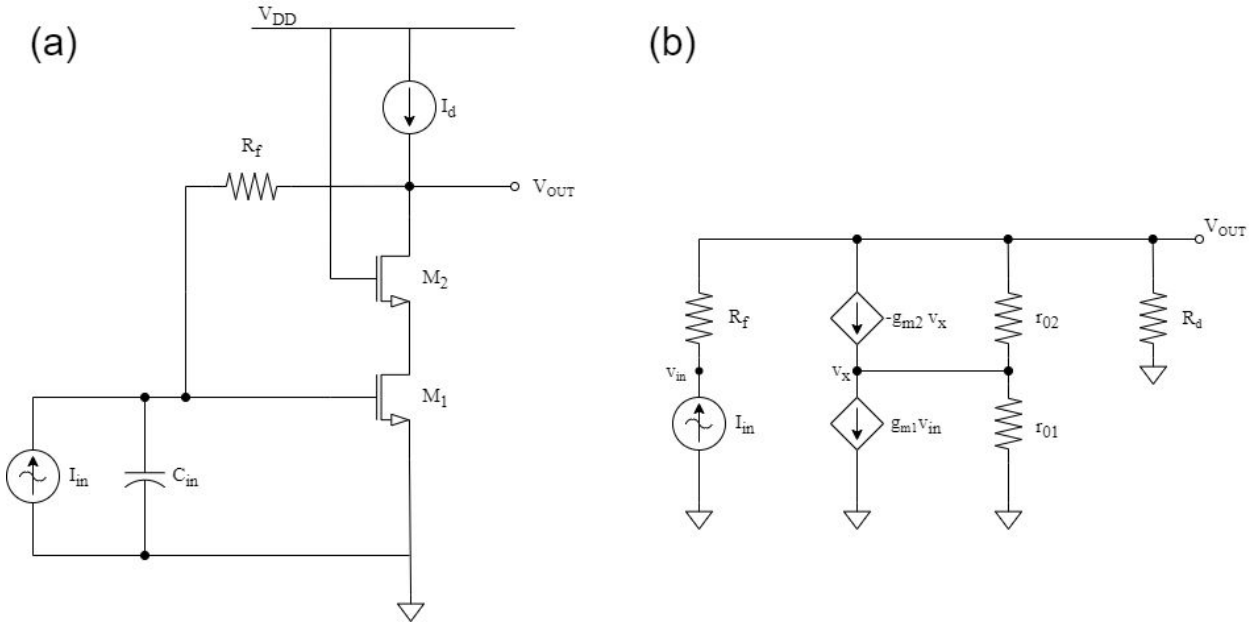

Figure 2: (a) Schematic of the input transimpedance stage. (b) Low-frequency small signal model of the circuit. This small signal model replaces the current source at the drain with a resistance, R_d

Figure 2 (b) shows the low-frequency small signal model of this stage. Observe that the ideal current source at the drain has been replaced with a resistance, R_d. The small signal model results in the following system of equations:

$$v_{in} = R_f I_{in} + v_{out}$$

$$I_{in} = -g_{m_2} v_x + \frac{v_{out} - v_x}{r_{0_2}} + \frac{v_x}{r_{0_1}}$$

Solving this equation simultaneously, gives us the following relationship:

$$\left[\frac{g_{m2}r_{o1}r_{o2}+r_{o1}+r_{o2}}{g_{m2}r_{o1}r_{o2}+r_{o1}}-g_{m1}R_f\right]I_{in}$$
$$=\left[\frac{g_{m1}-1}{r_{o2}}+\left(\frac{R_d+r_{o2}}{R_d r_{o2}}\right)\left(\frac{g_{m2}r_{o1}r_{o2}+r_{o1}+r_{o2}}{g_{m2}r_{o1}r_{o2}+r_{o1}}\right)\right]V_{out}$$

Since $g_{m2}\, r_{o1}\, r_{o2} \gg r_{o1}$, we can approximate the relationships as:

$$[1-g_{m1}R_f]\, I_{in} \approx \left[g_{m1}+\frac{1}{R_d}\right]V_{out}$$
$$\implies A_{iv}=\frac{V_{out}}{I_{in}} \approx R_d\left(\frac{1-g_{m1}R_f}{1+g_{m1}R_d}\right)$$

Under the same approximation, we can compute the input resistance to be

$$R_{in}=\frac{V_{in}}{I_{in}}=\frac{R_d+R_f}{1+g_{m1}R_d}$$

In the limit that the drain resistance is a current source (i.e. $R_d \to \infty$), we see that the gain approaches $-R_f$ and the input resistance approaches g_{m1}

$$\lim_{R_d\to\infty} A_{iv}=\lim_{R_d\to\infty} R_d\left(\frac{1-g_{m1}R_f}{1+g_{m1}R_d}\right)=-R_f$$

$$\lim_{R_d\to\infty} R_{in}=\lim_{R_d\to\infty}\frac{R_d+R_f}{1+g_{m1}R_d}=\frac{1}{g_{m1}}$$

Introducing the capacitors C_{in}, C_{gs1}, $C_{gd,1}$, C_{gs2}, and C_{gd_2} we can see that this system has 3 poles. Observe that shorting C_{gd2} gives us a non-zero output. Therefore, according to the generalized time constant method, the system must have at least one zero.

2.2. Simulation with an Non-Ideal Current Source

We implemented the current source (at the cascode drain) using a current-mirror topology, as described in Section 2.4. Using this circuit, we implement our TIA stage with parameters described by the table below. The choice of parameters is discussed in detail in Section 2.3.

R_f	I_d	M_1 Width	M_1 Length	M_2 Width	M_2 Length
950 Ω	1.45 mA	30 μm	50 nm	10 μm	50 nm

The resulting DC operating point parameters are described in the table below. The voltage drop across the non-ideal current source implies that the drain resistance is $342\ \Omega$.

g_{m1}	r_{o1}	g_{m2}	r_{o2}	Voltage drop across the current source
13.7mS	492.6 Ω	6.85mS	806.5 Ω	497mV

Using these values, we can estimate the trans-impedence gain as $A_{iv} = -723\ \Omega$ and the input resistance as $R_{in} = 227\ \Omega$. As seen in Figure 3, the estimate of the trans-impedence gain is very close to the simulated result.

We can estimate the 3dB bandwidth of this stage using the dominant pole approximation. To do this, we consider the zero-valued time constants for each of the capacitors.

Capacitor	Zero-valued Resistance	Resistance Value at DC	Time Constant	Explanation
$C_{in} = 500$ fF	$1/g_{m1}$	73.9 Ω	36.95 ps	Input resistance
$C_{gs,1} = 19$ f F	$1/g_{m1}$	73.0 Ω	1.39 ps	Input resistance
$C_{gd,1} = 4.19$ fF	$1/g_{m2}$	146.0 Ω	0.611 ps	Looking through M_2's source
$C_{gs,2} = 7.27$ fF	$r_{o1}\|\|1/g_{m2}$	112.6 Ω	0.819 ps	Looking through M_2's source and M_1's drain in parallel
$C_{gd,2} = 1.39$ fF	$R_d\|\|R_f\|\|g_{m2}r_{o1}r_{o2}$	704.2 Ω	0.979 ps	Output resistance of the cascode

As expected we the input capacitance significantly dominates the time constant. The total generalized time constant is 40.749 ps, which corresponds to an estimated bandwidth of 3.91 GHz. The AC simulations (as shown in Figure 3) yield a bandwidth of 2.85 GHz, demonstrating good agreement between the dominant-pole approximation and simulation results.

Our bandwidth is primarily limited by our non-ideal current source. This device has a relatively low resistance, preventing us from exploiting the low input-resistance benefits of this topology. Since this bandwidth falls below the requirements, we implement techniques such as shunt-peaking in the latter stages, to extend the bandwidth beyond 5 GHz. This is elaborated further in Section 3.

2.3. Optimizing Device Parameters

To address the bandwidth limitations, we aim to increase the transconductance of the bottom MOSFET g_{m1}. Firstly, we must scale these transistors to ensure that they're both in the saturation regime.

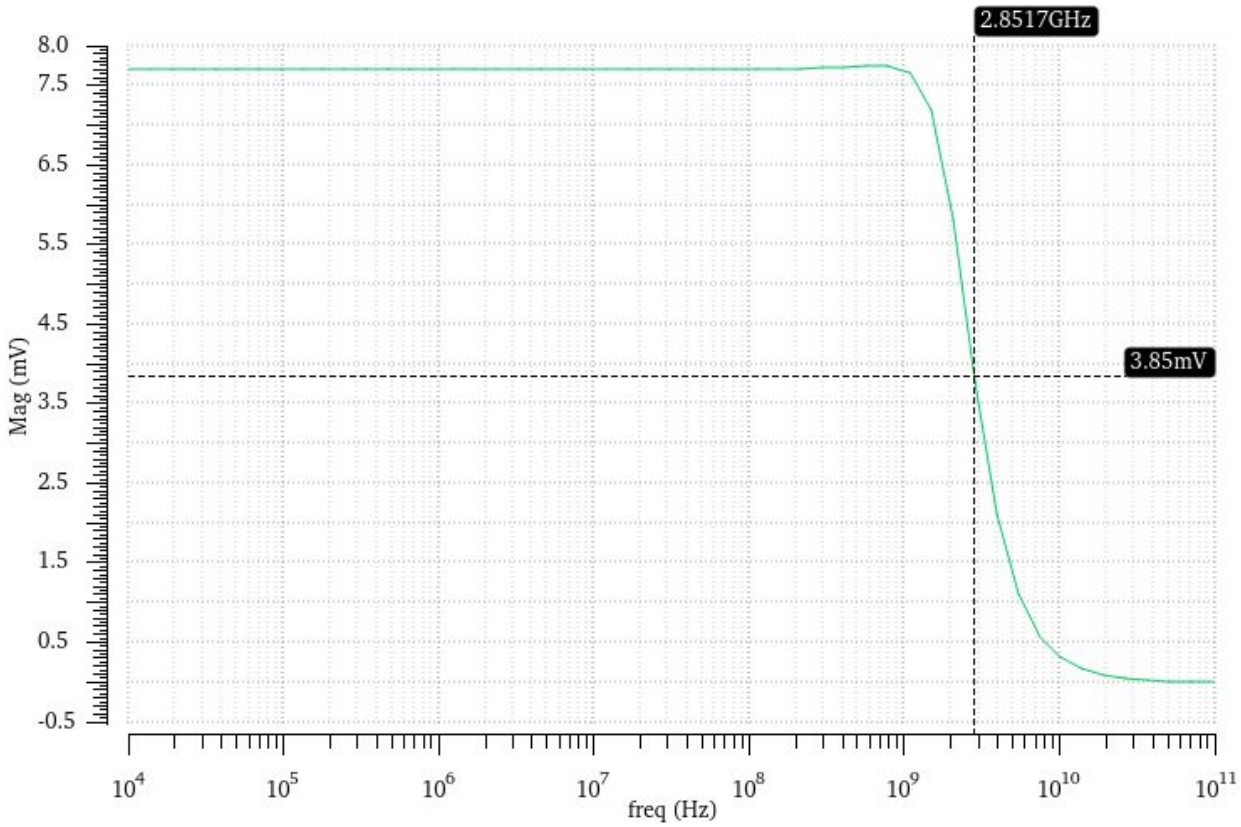

Figure 3: The frequency response (in millivolts) of the first stage corresponding to an input current of magnitude 10 μ A. For this stage, we are able to obtain a 3dB bandwidth of 3.85mV. We implement bandwidth-extension techniques in the latter stages to meet the minimum specifications.

Figure 4 plots the region of operation at DC for both transistors, as a function of their dimensions. The general trend is such that we must minimize the channel lengths and maximize the widths of the transistors to ensure that they're in saturation. In particular, the lengths of M1 and M2 must be less than about 300nm. At the same time, the widths must be greater than about 5 μ m.

Figure 5 shows the dependence of g_{m1} on the dimensions of M1 and the current through the cascode system. As expected, increasing the channel width and decreasing the channel length leads to higher g_{m1}. Varying the current has a relationship with g_{m1} that resembles a bell curve. We choose I_{ds} = 1.5mA, as this value is reasonably produced with the design described in Section 2.4. We choose smallest length of 50nm and a reasonably large width of 30 μ m.

We were cautious not to increase the width too much, as this would increase the parasitic capacitances. Secondly, while we aim to increase g_{m1} in order to increase the bandwidth, we must also consider that higher values of g_{m1} result in noisier transistors.

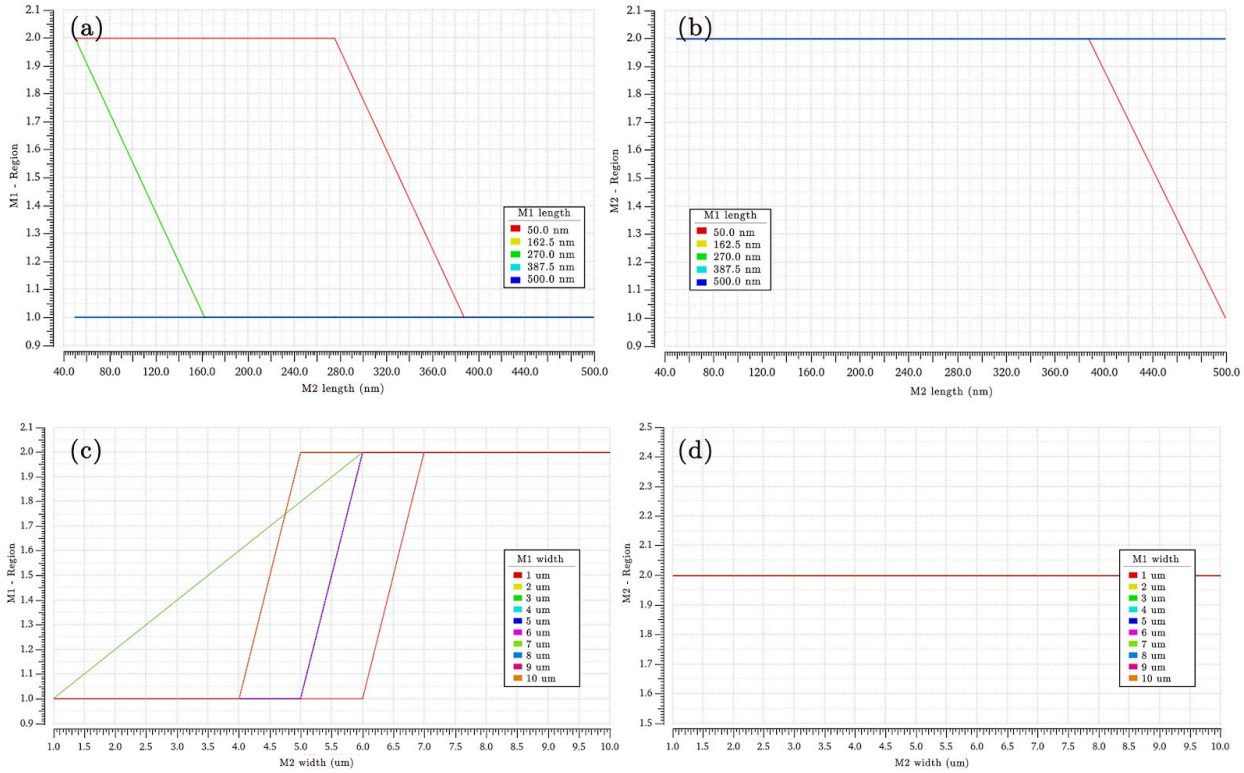

Figure 4: We vary the lengths (Panels a and b) and widths (Panels c and d) of both the transistors, and record the region of operation at DC. The 'region variable' is 1 when the device is in triode and 2 when it is in saturation.

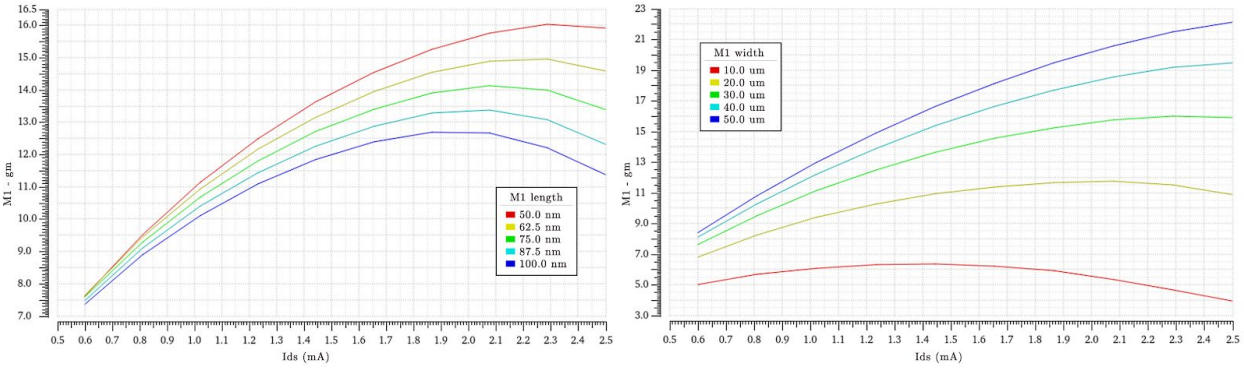

Figure 5: The transconductance, gm of the bottom transistor (g_{m1}) as a function of the current through the cascode and dimensions of M1 (the left panel varies length and the right panel varies the width). Observe that we've abided by the conditions that ensure that both MOSFETs are in saturation.

2.4. Current Source Circuit

The current source used within the TIA input stage is not ideal. To actualize it, we used an implementation of a current mirror circuit. The way it works is that there are two parts in the circuit: a generate circuit, and an amplify circuit. The amplify circuit generates a current of a certain magnitude, irrespective of the V_{DD} rail, that is based on the ratio of the left and right transistors, and then the amplify circuit takes that current and amplifies/reduces it by a certain factor that is also based on the ratios of the sizes of the transistors being used.

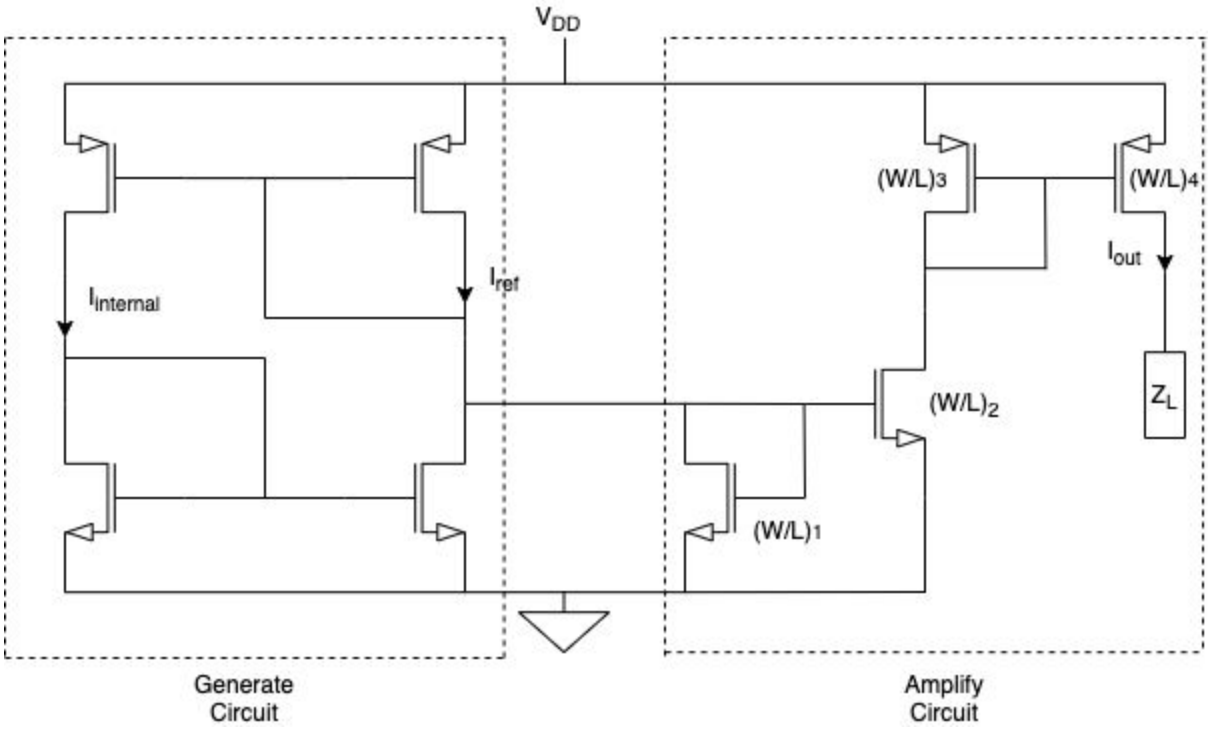

Figure 6: Schematic of the current mirror circuit that replaces the ideal current source

By using this schematic, we were able to generate 1.49066 mA, which is very close to the ideal amount of 1.5 mA. Getting the current as close to 1.5 mA as possible is important because the current dictates the bias point for the amplification stage, whose gain is very sensitive to the bias voltage.

Let I_{ref} be the current generated by the right side of the generate circuit, and let I_{out} be the current that results from the amplify circuit. If we define such currents to be this way, then the following currents hold true if all four transistors are in saturation and $\lambda \sim 0$:

$$I_{ref} = K \cdot I_{internal}$$

$$I_{ref} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH}) \qquad \text{in the long-channel model}$$

where $I_{internal}$ is the current generated by the left side of the generate circuit, and K is the ratio between the transistor dimensions of the left and right transistors of the generate circuit. We've written the long-channel current through the transistor; however we expect a similar relationship for transistors in the short-channel model. The equation for the amplify circuit is the following:

$$I_{out} = I_{ref} \cdot [[(\frac{W}{L})_2/(\frac{W}{L})_1]/[(\frac{W}{L})_4/(\frac{W}{L})_3]]$$

Where the transistor dimensions refer to the dimensions of the transistors in the amplify circuit, where the transistors are labeled. For clarification, the transistor dimension ratios are 176.9µ/1µ, 353.8µ/1u, 176.9µ/0.045µ, and 176.9µ/0.45µ for $(\frac{W}{L})_1$, $(\frac{W}{L})_2$, $(\frac{W}{L})_3$, and $(\frac{W}{L})_4$, respectively. For completion, the rest of the transistors in the generate circuit all have dimension ratios of 3931.11. As a result:

$$(\frac{W}{L})_1 = 176.9$$
$$(\frac{W}{L})_2 = 353.8$$
$$(\frac{W}{L})_3 = 3931.11$$
$$(\frac{W}{L})_4 = 3931.11$$

Upon running the simulation, we get an I_{ref} of 766.226 µA. Plugging in the values of the transistor dimensions into the equation for I_{out}, we expect an I_{out} of 1532.452 µA. Instead, we get 1.49066 µA.

3. Amplification Stage

The gain of the input stage is already significant at 770.12, so although theoretically we only need a gain of 6.49 to achieve a transimpedance gain of 5,000, we actually have a gain of 15.26 within the amplification stage alone. This happened as a result of fine-tuning the entire circuit, mainly adjusting the resistors' values, towards the end of the design of the circuit in an attempt to help us achieve a 100 mV swing.

Regardless, our topology was designed with bandwidth in mind. As a result, we decided to go with a simple cascode topology because it is the most effective at eliminating the Miller effect and maintaining a higher bandwidth. We implemented the same transistor dimensions as in the TIA stage, as these were designed to maximize the transconductances.

Moreover, inherent within cascode is its ability to also achieve a high gain. Since there is a fundamental tradeoff here between gain and bandwidth, and our need for gain was not significant

(our original assumption was a gain of 50), we decided to change the R_{UP} to a simple resistor in order to significantly reduce the gain and the time constant of the load, thereby leading to a higher bandwidth.

$$\textit{Gain of stage 1: } A_1 = -g_{m1}(g_{m2}r_{o2}r_{o1} \| R_{UP})$$
$$\textit{Gain of stage 2: } A_2 = -g_{m3}(g_{m4}r_{o4}r_{o3} \| R_{UP})$$

where $R_{UP} = R_{2a}$ for A_1 and $R_{UP} = R_{2b}$ for A_2. We've ignored the inductors for this low-frequency calculation.

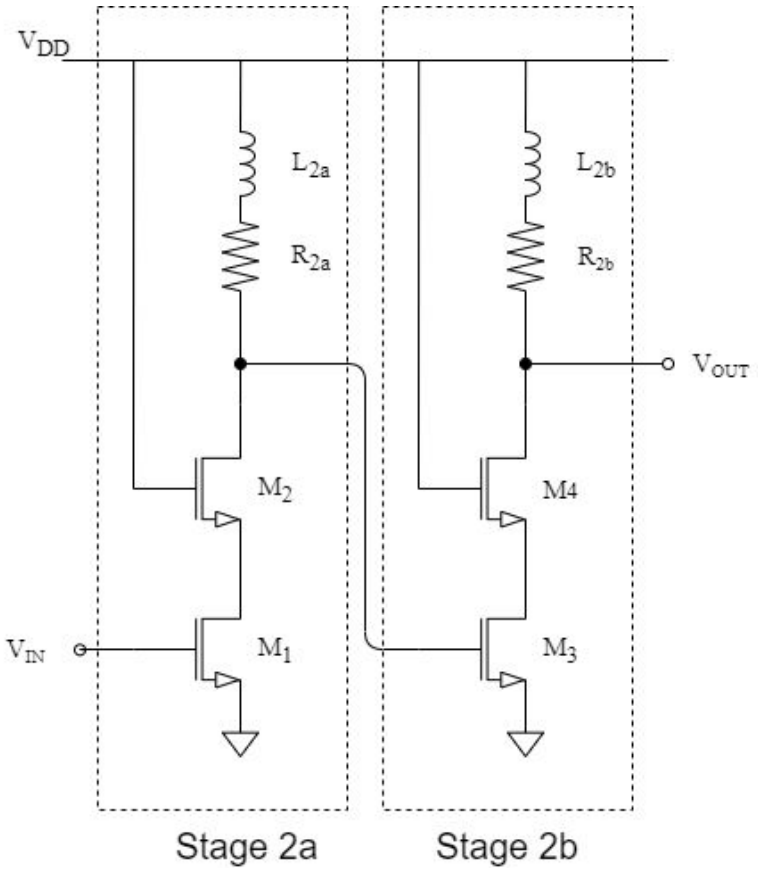

Figure 7: Schematic of the amplification stage broken down into two different stages

In order to extend the bandwidth, we used the shunt-peak method. As shown in Figure 8 the values of the inductors were swept to find the value which resulted in the largest bandwidth and flattest response. We settled on $L_{2a} = L_{2b} = 15$nH, which resulted in a bandwidth of 8.2 GHz and a peak of 0.87 dB.

The table below summarizes the amplification stage's device parameters

Parameter	Stage 2A	Stage 2B
R_{UP}	300 Ω	300 Ω
Transistor Width	30 µm	30 µm
Transistor Length	45 nm	45 nm
Shunt-Peak Inductance	15 nH	15 nH

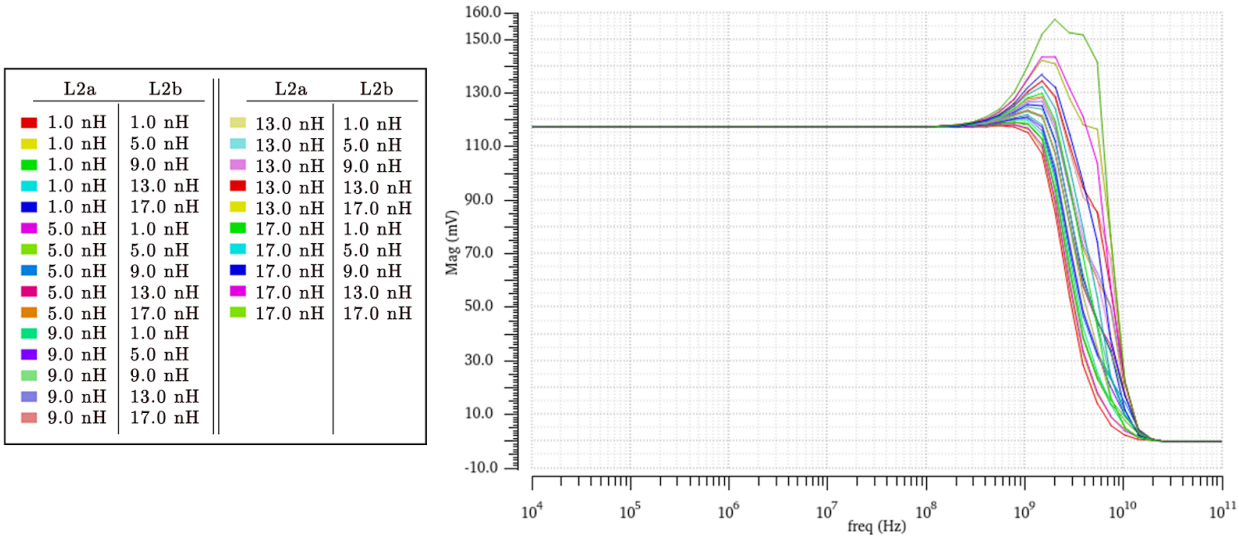

Figure 8: Frequency response while sweeping the values of the shunt-peak inductors at each amplification stage. As shown in the schematic, L_{2a} corresponds to the inductor in the left branch and L_{2b} corresponds to the one in the right branch.

These parameters result in the DC operating point values as below:

Parameter	Stage 2A	Stage 2B
Bottom Transistor Transconductance (g_{m1}, g_{m3})	16.0918 mS	14.2602 mS
Top Transistor Transconductance (g_{m2}, g_{m4})	15.3252 mS	14.0584 mS
Bottom Effective Resistance (Ω) (r_{o1}, r_{o3})	512.295 Ω	636.94 Ω
Top Effective Resistance (Ω) (r_{o2}, r_{o4})	342.934 Ω	466.418 Ω

Using the equations above, we calculate the gain of Stage 2a to be 4.344 and of Stage 2b to be 3.99. Figure 9 shows that gain of stage 2a is 6.1 dB, which approximately equals 4.07. Likewise, from Figure 9 we see that the gain of stage 2b is around 6 dB or 3.98. These values agree very closely with the analytical results.

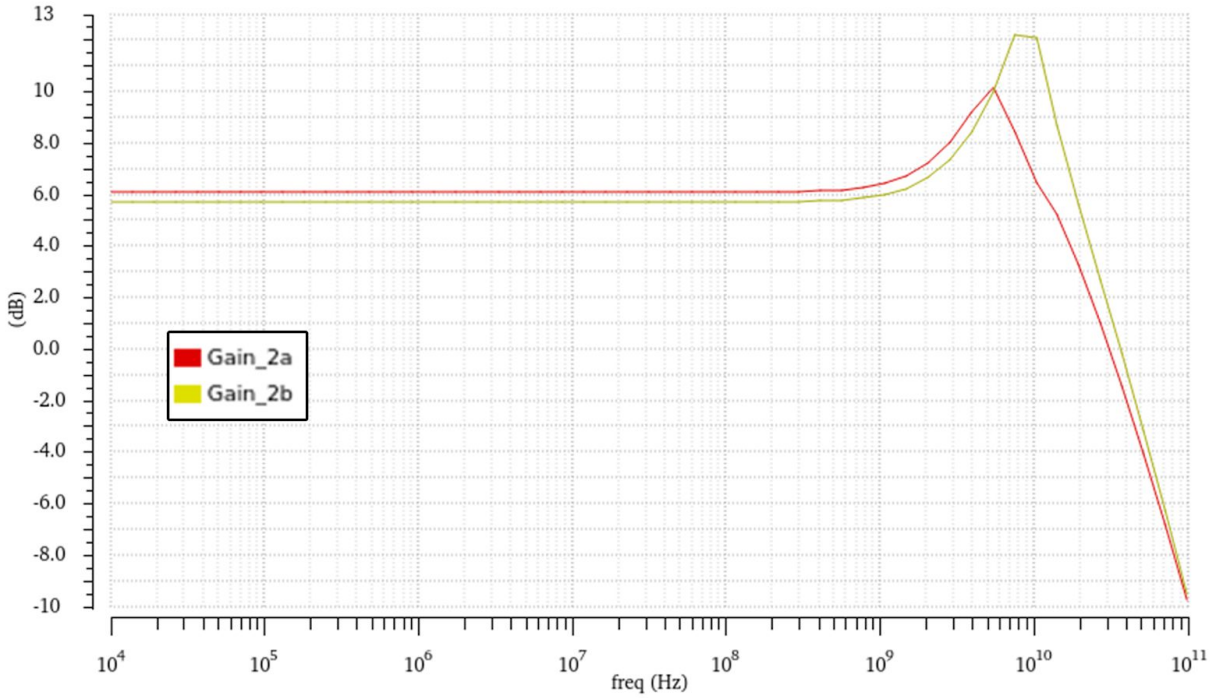

Figure 9: The frequency response of the individual gains from Stages 2a (red) and 2b (yellow). We see that the gain of stage 2a is about 6.1 dB and that of 2b is about 6 dB.

Finally, Figure 10 gives us important information on the characteristics of the system, thereby proving that we have satisfied the design specifications. It shows us the entire transimpedance gain magnitude of around 40.7 dB or 11,724.65 Ω, which is more than double the required gain. Furthermore, the 3dB bandwidth of the system is about 7.77 GHz. This is all accomplished with a peak height of 0.8 dB, which is within the 1dB limit.

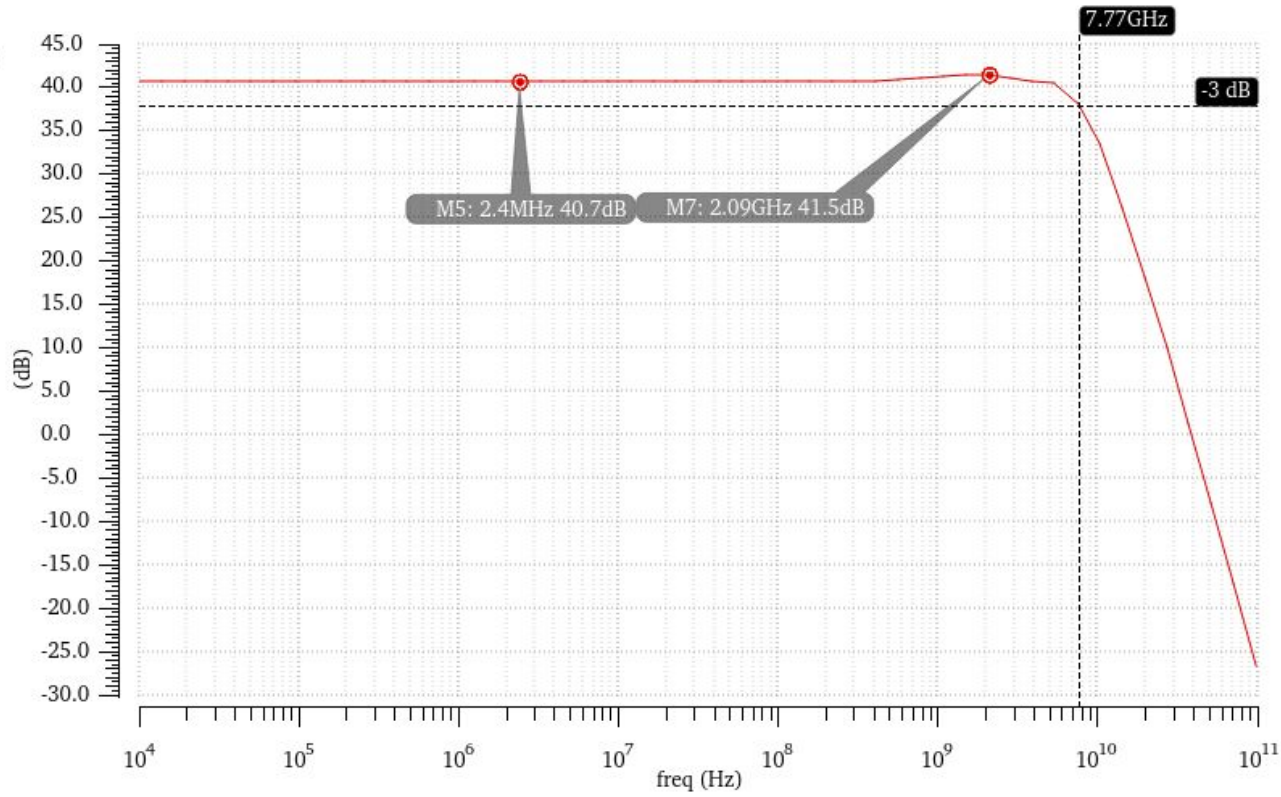

Figure 10: Plot of the total transimpedance gain, between the photodiode input and the output of the second stage of the amplification stage. The DC gain is about 40 dB with a bandwidth of 7.77 GHz, and a peak of 0.8 dB.

4. Differential Stage

The bandwidth and transimpedance gain have been met; however, we still need to convert it into a differential signal. We do this by first implementing the differential circuit that we have seen in class with an ideal current source to suppress the common mode. We bias the right side with a particular voltage so that the DC operating point is identical to the one at the input by using voltage division with $R_{div,1}$ and $R_{div,2}$. The idea here is that we will keep the right side in the saturation regime, and it's current, and thus output N, will be a function of the AC component of the input because the current going through the tail must be constant. Within this particular schematic, we have decided to leave in the ideal current source despite design specifications because attempting to implement a current source by using a MOSFET at the tail of the circuit has proven to be so far unfruitful due to our inability to get the MOSFET to operate in the saturation regime. We suspect this may be due to the low V_{DD} overhead we may have.

The gain of the differential amplifier is similar to that of the common source topology:

$$A = -g_m(r_o \| R_{UP})$$

where

$$g_m = 8.069 * 10^{-3}$$
$$r_o = 108,459.87$$
$$R_{UP} = 1,000$$

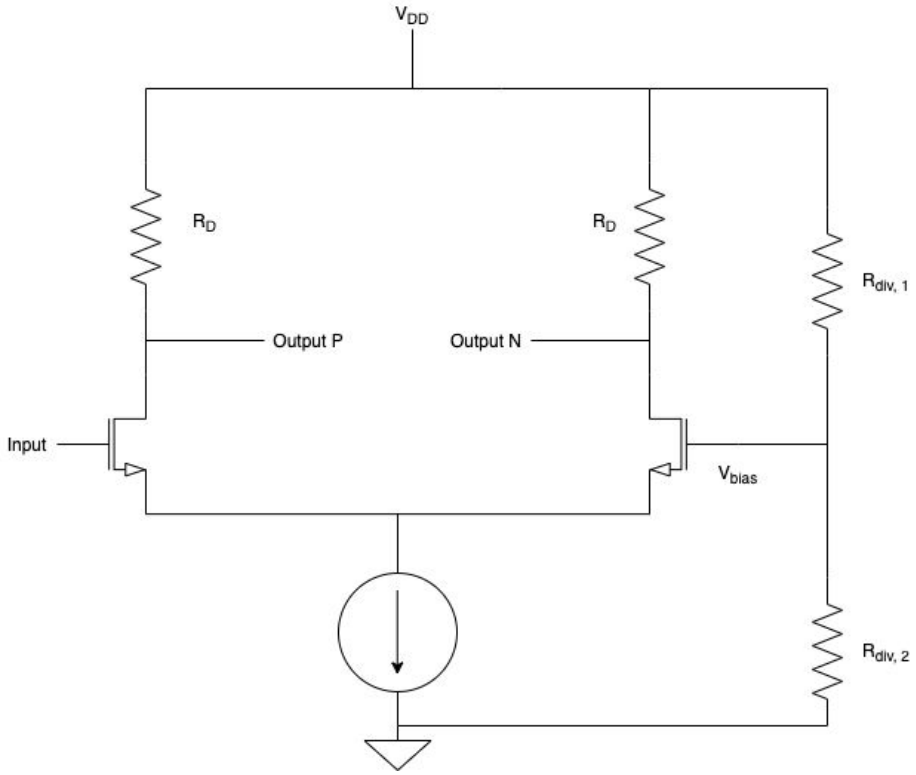

Figure 11: The schematic of our differential output stage

This means the differential gain should be around 8 and the differential swing to be:

$$\text{Differential swing} = 11,700 * 8 * 10 * 10^{-6} = 0.936 \text{ V}$$

Thus, the expected differential swing should be at around 0.936 V, but our simulation gives us a swing of about 500 mV, which will further be significantly reduced once we connect the bypass capacitance and load resistance.

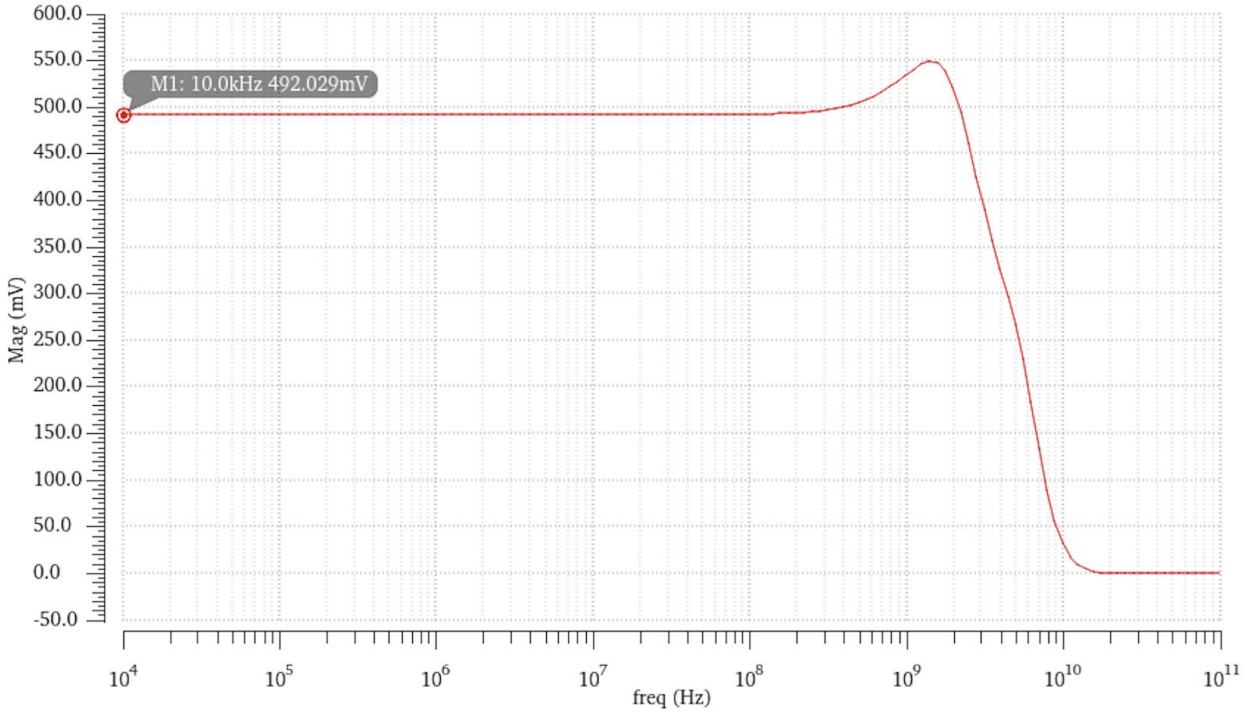

Figure 12: Plot of the differential swing without any load

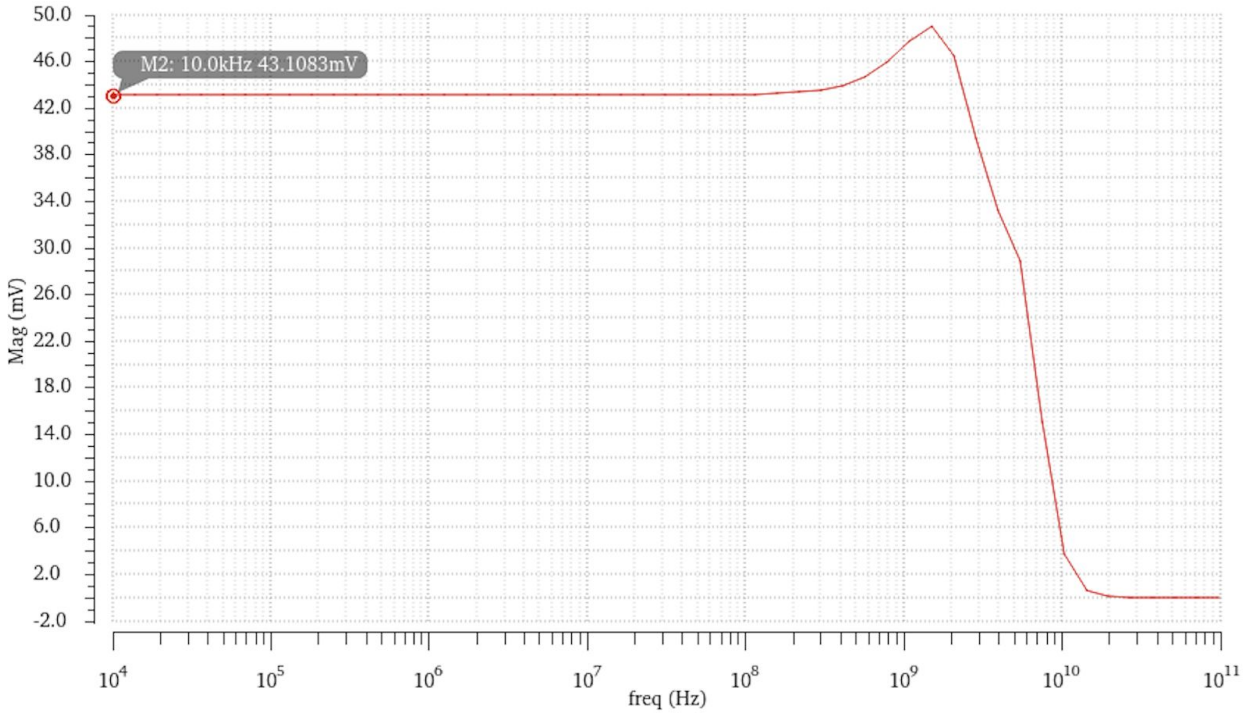

Figure 13: Plot of the differential swing with the lo-pass load

Figure 13 shows that when the bypass capacitors and load resistances are attached, the differential swing experiences a reduction of over 10.

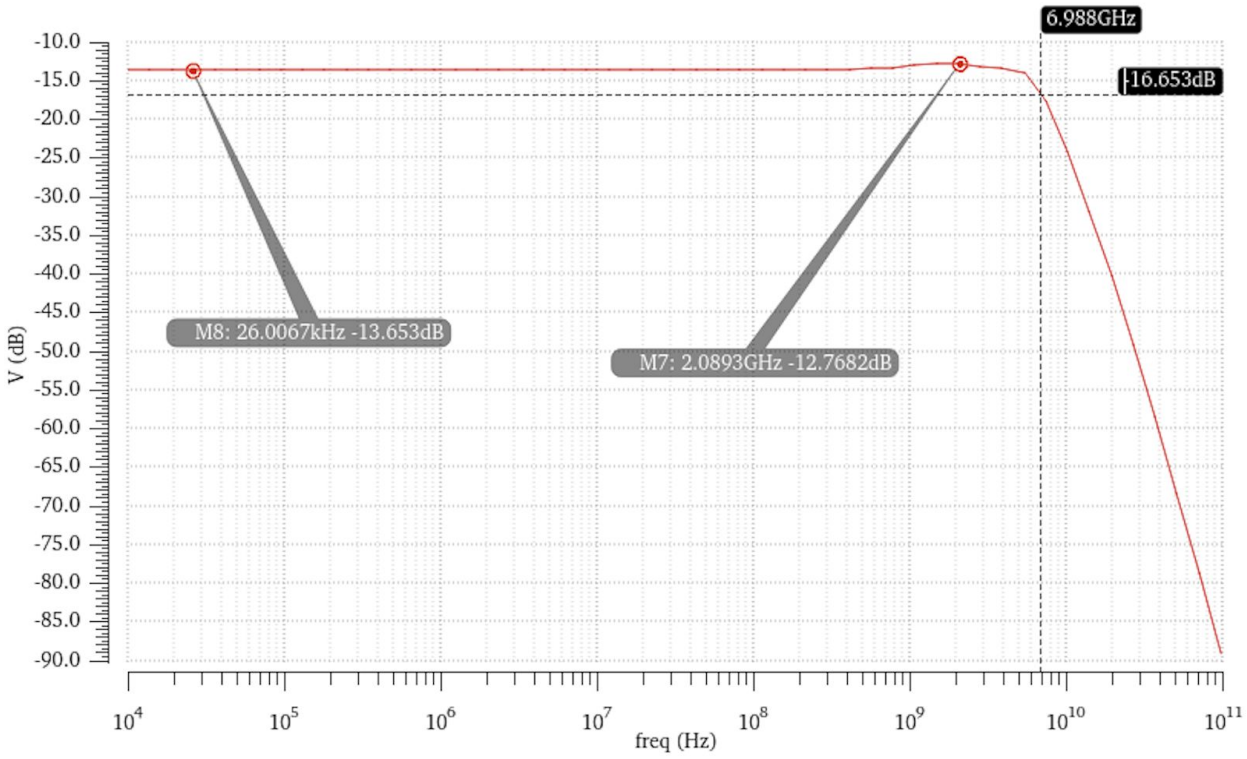

Figure 14: Plot of the differential swing on a logarithmic scale, with 3dB point shown

Figure 14 shows a transimpedance gain of around -13.653 dB, which is about the same as ~ 4.3 mV. In other words, the plot also represents our final signal with a voltage swing of 43 mV. The 3dB point is 6.988 GHz, thus satisfying our bandwidth specification.

Compared to our input current of 10 μA, this would mean we ultimately had a gain of about ~ 4,300. Even though we had a large gain from our second stage, we're significantly limited by the gain of our differential stage. The source of this unusual behavior is probably because our differential stage is not perfect. We were unable to bias the transistors to have large transconductances while maintaining them they're in saturation.

Furthermore, we can see the peaking of the system is less than 1 dB, as the peak is at -12.7682 dB, pass band is at -13.653 dB, resulting in a difference of 0.8848 dB.

5. Noise Analysis

Figure 15 shows the noise analysis between 1GHz and 5GHz (a) before and (b) after the differential stage.

After the differential stage, we have a maximum noise level of 126.49 $f(V)^2/Hz$. Using the differential gain of 4.31kΩ, this gives us a maximum input referred noise of 82.5 pA/$\sqrt{Hz}$.

Before, the differential stage, we have a maximum noise level of 997.26 $f(V)^2/Hz$. However, we also have a larger gain of 11.73kΩ, which gives a maximum input referred noise of 85.13 pA/$\sqrt{Hz}$. This implies that the differential stage adds very little noise to the system.

The table below shows the top-six contributors of noise in the system.

Device	Noise Source	Noise Contribution	Percentage of Total
stage1_M1	Thermal Noise	2.299×10^{-13}	23.05 %
curr_src_PM3	Thermal Noise	2.176×10^{-13}	21.82 %
curr_src_PM2	Thermal Noise	1.844×10^{-13}	18.50 %
curr_src_PM3	Current Noise	8.816×10^{-14}	8.84 %
curr_src_PM2	Current Noise	6.052×10^{-14}	6.07 %
curr_src_NM3	Current Noise	5.563×10^{-14}	5.65 %

6. Conclusion and Final Remarks

To conclude, we created a transimpedance amplifier that consists of three main stages: input, amplification, and output. The design of our input stage is based on the input stage seen in problem set 3, but changed to a cascode version to increase the bandwidth. As a result, the gain of our input stage is pretty, allowing us to focus more on the bandwidth aspect of the circuit for the amplification stage. Within the amplification stage, we have two back-to-back cascode stages that give us a small enough gain to give us a transimpedance gain of over 5,000, and a bandwidth that gets us over 5 GHz. Lastly, our differential stage is based on a topology we have seen in class, but unfortunately does not behave in a manner we would expect to due to how we implemented the circuit given the design limitations and tools that were available at hand. Based on the results that we have shown before and after the differential stage, it is safe to say that we do not have a very robust differential stage, and that improvement of the circuit would have to focus on drastically improving the differential stage; this most likely would be done by overhauling the entire stage and implementing a completely different design. Nonetheless, we were able to satisfy most of the design requirements put forth by the project.

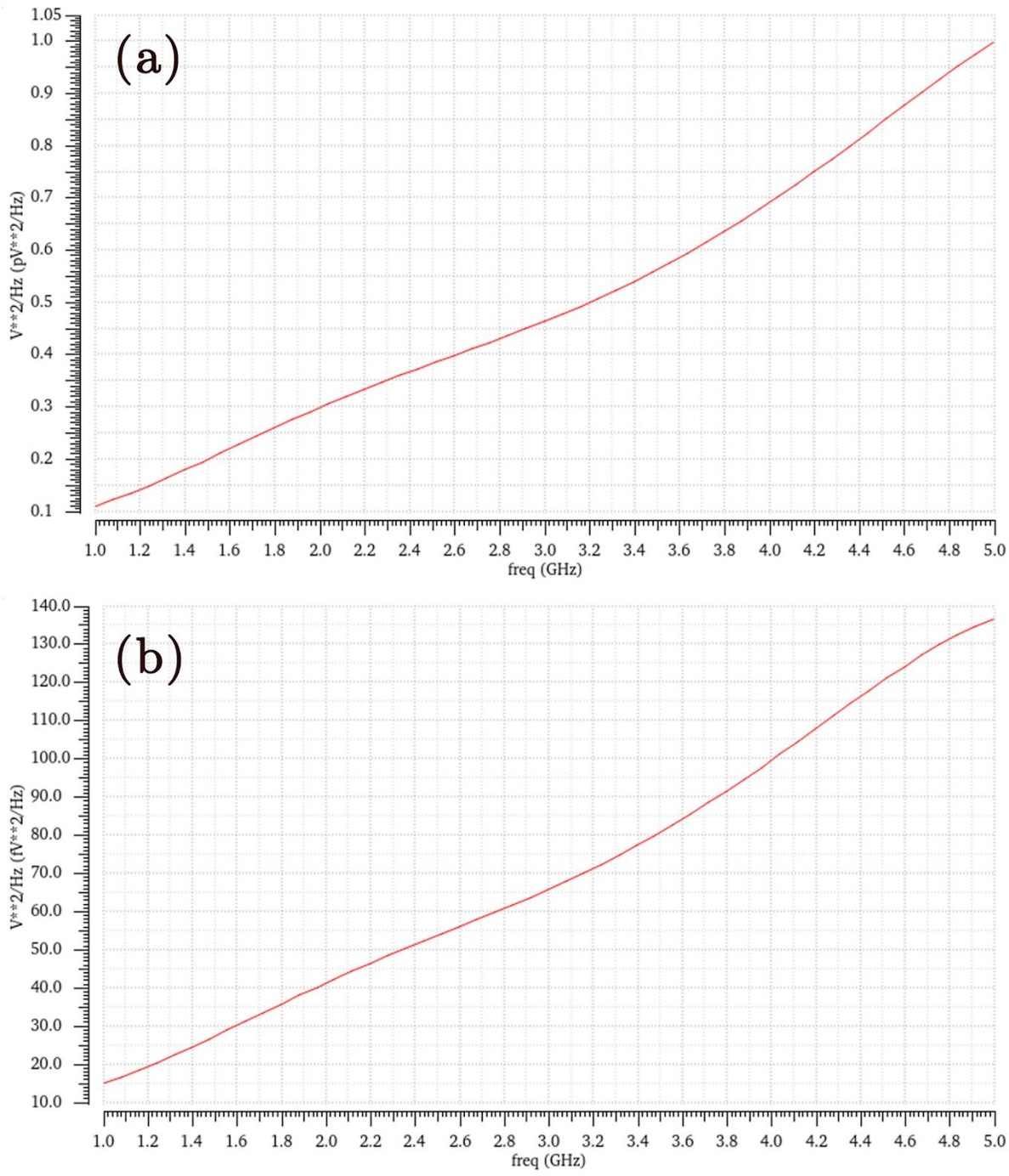

Figure 15: The noise spectral density between 1GHz and 5GHz (a) before and (b) after the differential stage.